In the Specification

IFW SENT

Please amend the ~~second full~~ third paragraph on page 8 as follows:

IDC-A1,AMD

The differential pair of transistors Q1, Q2 are connected to a first latch 710 and second latch 720 through output lines designated as b and b. The dual connection of b and b, provides twice the voltage potential swing as a single input would provide. Connecting only a single one of the outputs b, b, to the latches 710, [710] 720 provides half the available signal swing, which is harder to detect.